IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	09/767,379 Confirmation No. 2354
Applicant	:	Bertram Gunzelmann, et al.
Filed	:	January 22, 2001
Title	:	Acquisition Method and Apparatus for Carrying Out the Method
Group Art Unit	:	2637
Examiner	:	Sam K. Ahn
Docket No.	:	GR 98 P 8060 P
Customer No.	:	24131

DECLARATION UNDER 37 C.F.R. § 1.131

I, Bertram Gunzelmann, an inventor of the invention described and claimed in the instant application hereby declares that:

The invention of the above-identified application was "conceived" and "reduced to practice" in Germany, a WTO member country, at least as early as February 16, 1998.

I personally wrote an Invention Disclosure (Erfindungsmeldung) on December 2, 1996, and then submitted it to my supervisor, Dr. Hartmann, at the Siemens department HL DC E, who confirmed receipt on December 2, 1996.

Enclosed, as corroborating evidence is the Invention Disclosure (*Erfindungsmeldung*).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

_____ _____

Bertram Gunzelmann Date

(2)

Vertraulich!
An
Siemens AG

ERFINDUNGSMELDUNG
Bitte verschlossen weitersenden!

Aktenzeichen der GR
96 E 8129 DE

Ich/Wir (Vor- und Nachname des/der Erfinder[s] - weitere Angaben und Unterschrift[en] letzte Seite)
Bertram Gunzelmann

Datum der Ausfertigung:
2.12.1996

melde[n] hiermit die auf den folgenden Seiten vollständig beschriebene Erfindung mit der Bezeichnung:
Schnellere Akquisition eines CDMA Empfängers durch verbesserten Korrelator

I. An Vorgesetzten des/der Erfinder[s]

Eingang am:

Herrn/Frau Dr. Hartmann HL WS PD
(Dienststelle)

mit der Bitte, die nachstehenden Fragen zu beantworten:

a) Wann ging die Erfindungsmeldung bei Ihnen ein? →

b) Geht die Erfindung auf öffentlich geförderte Arbeiten zurück?

[x] nein [ ] ja, Projekt (Vorhaben): _____

c) Bitte bei Zuständigkeit auch zu Ziffer III. Stellung nehmen.

2.12.96 _____
(Datum) (Unterschrift des Vorgesetzten)

Ab Eingang läuft gesetzliche Frist

II. Bitte wegen gesetzlicher Frist sofort weiterleiten

Eingang am:

An ZFE GR (Patentabteilung)

zur weiteren Veranlassung.

GR ZD VM Mch M
Eing. 3. DEZ. 1996
GR

III. An Geschäftsgebiets- bzw. Abteilungsleitung

Eingang am:

Herrn/Frau _____
(Dienststelle)

Zur Entscheidung bzw. Empfehlung über Inanspruchnahme (Zutreffendes bitte ankreuzen!):

[ ] Die Erfindung sollte unbeschränkt in Anspruch genommen werden.
Kosten trägt (Organisationseinheit): _____

[ ] Die Erfindung kommt für eine Behandlung als Betriebsgeheimnis in Betracht.

[ ] Die Erfindung kommt evtl. für Auslandsanmeldungen in Betracht.
Länder: _____

Vermerke der ZFE GR

[ ] Die Erfindung wird voraussichtlich nicht benutzt.
Bei Freigabe wäre aber ein Benutzungsrecht wünschenswert.

NL

[ ] Die Erfindung kann dem/den Erfinder[n] vorbehaltlos freigegeben werden.

HL 04

[ ] Die Erfindung betrifft nicht unser Interessengebiet. Es sind noch folgende Dienststellen zu befragen: _____

Dringlichkeitsvermerk

(Datum) (Unterschrift der Geschäftsgebiets- bzw. Abteilungsleitung)

IV. Zurückerbeten an ZFE GR

1. Welches technische Problem soll durch Ihre Erfindung gelöst werden?
2. Wie wurde dieses Problem bisher gelöst?
3. In welcher Weise löst Ihre Erfindung das angegebene technische Problem?

1. Schnellere Akquisition eines CDMA Empfängers
2. Anlage
3. Anlage

4. Zur weiteren Erläuterung sind als Anlagen beigefügt:

x Blatt der Darstellung eines oder mehrerer Ausführungsbeispiele der Erfindung;

x Blatt zusätzliche Beschreibungen (z.B. Laborberichte, Versuchsprotokolle);

_____ Blatt Literatur, die den Stand der Technik, von dem die Erfindung ausgeht, beschreibt;

_____ Blatt sonstige Unterlagen:

Improved CDMA Acquisition Receiver

Abstract
An improved method of code and doppler searching in a digital direct sequence spread spectrum system such as Global Positioning system (GPS)

Background of the invention
Radio navigation systems are used for providing useful geographic location and time information. The GPS navigation system relies of satellites which are constantly orbiting the globe, so allowing to derive precise navigation information including 3-dimensional position, velocity and time. Normally, reception of signals from 4 satellites is required for precise location determination in 4 dimensions (latitude, longitude, altitude, time). Once the receiver has measured the respective signal propagation delays, the range to each satellite is calculated by multiplying each delay by the speed of light. Then the location and time are found by solving a set of 4 equations incorporating the measured ranges and the known locations of the satellites. The highly precise capabilites of the system are maintained by means of on board atomic clocks for each satellite and by ground tracking stations which continuously monitor and correct satellite clock and orbit parameters.

Each GPS satellite transmits 2 direct-sequence-coded spread spectrum signals at L-band: a L1 signal at a carrier frequency of 1.57542 GHz and a L2 signal at 1.2276 GHz. The L1 consists of 2 phase-shift keyed (PSK) spread spectrum signals modulated in phase quadrature: the P-code signal (P for precise) and the C/A-code signal (C/A meaning coarse/acquisition). The L2 signal contains only the P-code signal. The P and C/A codes are repetitive pseudorandom sequences of bits (called Chips in spread spectrum parlance) which are modulated onto the carriers. The clocklike nature of these codes is utilized by the receiver in making time delay measurements. The codes for each satellite are unique, allowing the receiver to distinguish between signals from the various satellites even though they are all at the same carrier frequency. Also modulated onto each carrier is a 50 bit/sec data stream (different for each satellite) which contains information about system status and satellite orbit parameters, which are needed for the navigation calculations. The P-code signals are encrypted, and available only to classified users. The C/A signal is available to all users.

The operations performed in a GPS receiver are for the most part typical of those performed in any direct-sequence spread spectrum receiver. The spreading effect of the pseudorandom code modulation must be removed from each signal by multiplying by a time-aligned, locally-generated copy of it's code, in a progress known as despreading. Since the appropriate time alignment, or code delay, is unlikely to be known at receiver

startup, it must be searched for during the initial acquisition stage. Once found, proper code time-alignment must be maintained during the tracking phase of receiver operation, as the user and the satellites move around. A mechanism for maintaining this alignment is called a delay-locked loop.

Once despread, each signal simply consists of a 50 bit/sec PSK signal at some low intermediate frequency. This frequency , is somewhat uncertain due to the Doppler effect caused by the relative movement between satellite and user, and due to receiver local clock error. During initial signal acquisition the uncertainty frequency range must be searched for, since it is usually unknown prior to acquisition. Once the Doppler frequency is approximately determined, carrier demodulation can consider this by digital processing means.

To accomplish the functions described above, most parts are performed by digital means. After high speed 1 bit A/D convertion a DSP is used for loop filtering, data detection, bit timing recovery. Decorrelation is done with special acceleration hardware, which is explained later. The navigation computations are mainly performed using a microprocessor.

An drawback to the processing methods employed in current GPS receivers is the long time needed for initial acquisition. As mentioned above, before the 4 satellite signals can be tracked they must be searched for in a 2-dimensional search space, whose dimensions are code delay and frequency. Typically if there is no knowledge of a signals location within this search space, as would be the case after a receiver 'cold start', a large number of code delays (1023 for the C/A code) and Doppler frequencies (approx. 20) must be searched. Thus for each possible satellite signal, up to 20.000 locations must be examined. A conventional correlator receiver takes 1 ms for searching one location.

In the acquisition process a reliable decision for or against 'synchronisation' is needed. As the SNR of the examined locations is very low due to received signal power a postprocessing of the correlator output signal is still needed. In the acquisition postprocessing every location is examined several times, the results of the respective locations are processed, e.g. by accumulating the received power. This increases the SNR and as a consequence the detection probability. For this reason the number of examined locations is even times greater as the above mentioned number of 20.000.

It is apparent from the above discussion that GPS receivers with a conventional correlator architecture are limited to long acquisition times. Most prior receivers perform the GPS signal search in a sequential manner. The usual procedure is for the receiver to make a guess as to the correct frequency bin, setting the digital frequency shifter accordingly. Then for the frequency bin all code delays are examined for presence of

The input signal coming from the chip matched filter is taken at a frequency of 1 Mhz and put to the FIFO. The FIFO output value is stored short-termed and the FIFO content is written to the first address of the RAM. After this the adress pointer is incremented and the FIFO is loaded again with a new 32 bit word. After shifting the FIFO content the short-term stored value is input to the FIFO and the content is stored at the currently pointed adress. This step is repeated until all 32 RAM words are shifted. Therefore the procedure is running at a clock of 32 MHz.

The 32 bit data from the input signal and the Gold code are compared at a rate of 32 MHz by a simple XOR operation resulting in a new 32 bit word. The following bits summator calculates the number of '1' which are the agreements of Gold code and input signal.

The bits summator of **fig. 5** has to work at the same clock of 32 Mhz. This 32 bit adder consists of simple 1 bit adders in the first stage, 2 bit adders in the second stage, 3 bit adders in the 3rd stage, 4 bit adders in the 4th stage and 5 bit adders in the 5th and last stage resulting in a 6 bit word. So internally the clock rate has to be 5 times higher. Because this operation is not time critical the addition operations can be performed pipelined for every stage, thus reducing the internal clock rate to the external clock rate. For this realization the output of each adder has to be latched. After passing the result from one stage to the next, the prior stage can be used again for the next input values.

To receive the number of agreements 32 cyles of the bits summator have to be accumulated. Hence this block is also running at 32 MHz. In order to receive the correlation result the accumulated number of agreements has to be processed by 1023-2*Accumulator.

After correlating the inphase and the quadrature components both values are squared and added in order to obtain the signal power. To reduce the quantization range to 6 bit the square root of the signal power is taken. The result is added to the corresponding adress of acquisition RAM. This accumulation is done M times in order to obtain sufficient signal power.

signal. If no signal is found, the frequency shifter is adjusted to the next frequency and the process is repeated.

For a given code delay/Doppler frequency trial the C/A signal is digitally mixed with a sinusoid/cosinusoid whose frequency is equal to the current Doppler guess and is multiplied by the locally generated C/A code. The resulting signal is filtered by a filter whose bandwidth is commensurate with the frequency search interval Δf of the location. If the desired signal is present in the location being searched, after postprocessing the result will be compared to a threshold. If the result is greater than the threshold, the signal is deemed present in the current bin. Otherwise the signal is deemed absent, and the search proceeds to the next bin.

Detailed description

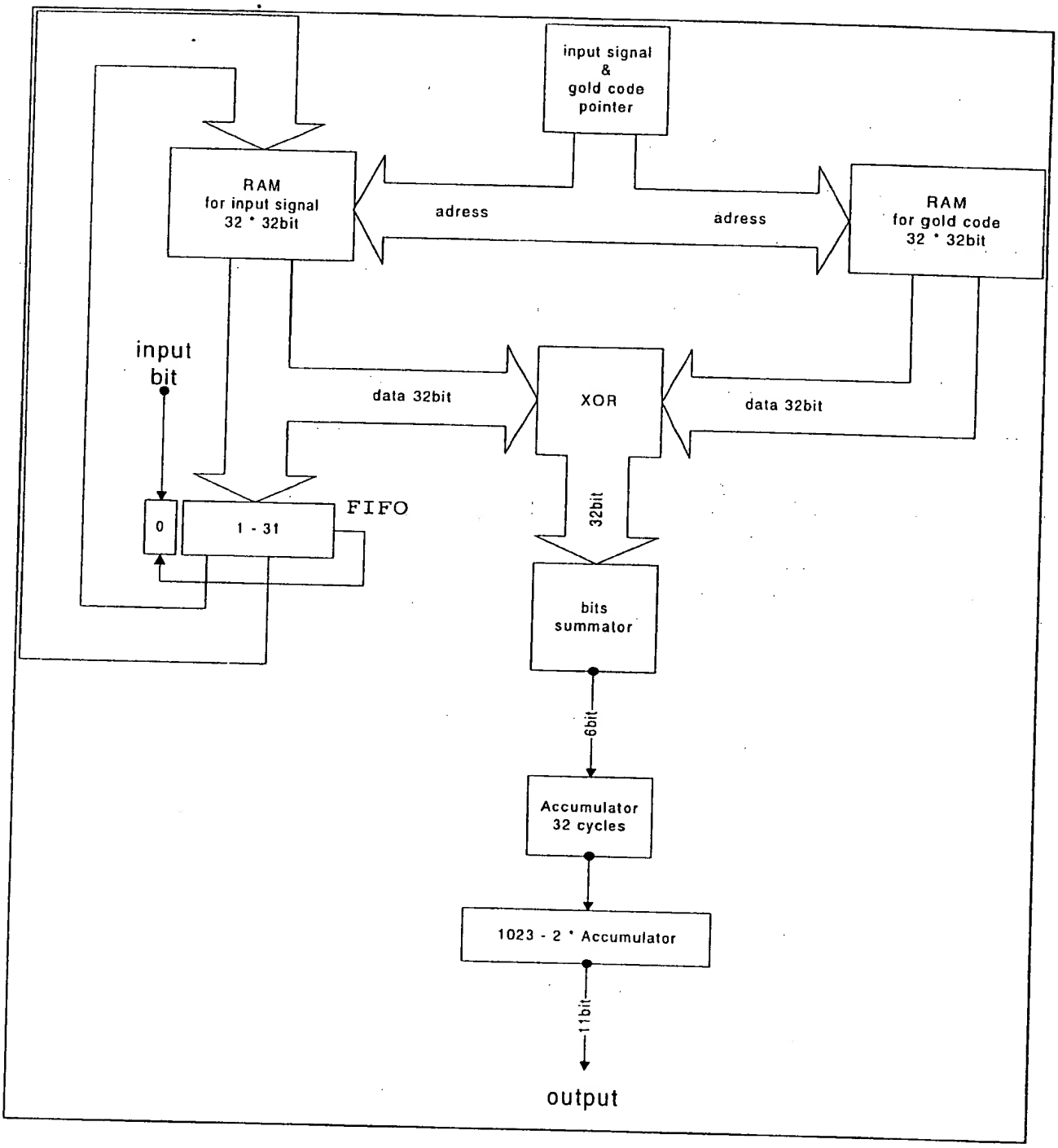
Fig. 1 illustrates the primary functional blocks of the GPS acquisition receiver as implemented in accordance with the invention. This figure is shown to employ an antenna that is suitable of receiving the L1 signals broadcast by the GPS satellites. The antenna output is connected to a down converter. The output of the down converter is an very low intermediate frequency near to the baseband, containing the frequency translated satellite signals. The resulting inphase and quadratur components of the signal are sampled with 1 bit resolution with a frequency of OSR*1MHz, where OSR is the oversampling ratio. 26 is a possible value for OSR. The OSR samples are filtered using a chip-matched filter and fed to the digital preprocessor at a rate of 1 MHz and 1 bit resolution.

In **fig. 2** the principle of the digital preprocessor is presented more in detail. The 1 bit samples are frequency shifted by digital means depending on the frequency location to be searched. The frequency shifter is depicted in **fig. 3**. The sinus and cosinus are approximated with 1 bit resolution taking the values 1 or 0.

After multiplying with the locally generated spreading sequence the samples are acummulated over 1023 chips and the signal power is calculated. Then the square root is taken and for a particular location the signal power is accumulated M times.

As indicated by the introduction above several locations have to be searched in the time and frequency domain. In the time domain there are 1023 bins to be searched due to the Gold code spreading sequence of period 1023. This implies that in the time domain a resolution of +/- a half chip is achieved. In order to accelerate the acquisition process a new correlator architecture is presented in **fig. 4**. This architecture has the capability to search all 1023 bins of the time domain parallel in 1 ms.

Depending on the satellite a 1023 bit Gold code is generated by a DSP and stored in the 32*32 bit RAM. This memory is kept fixed for the search time. The signal RAM has the same size.



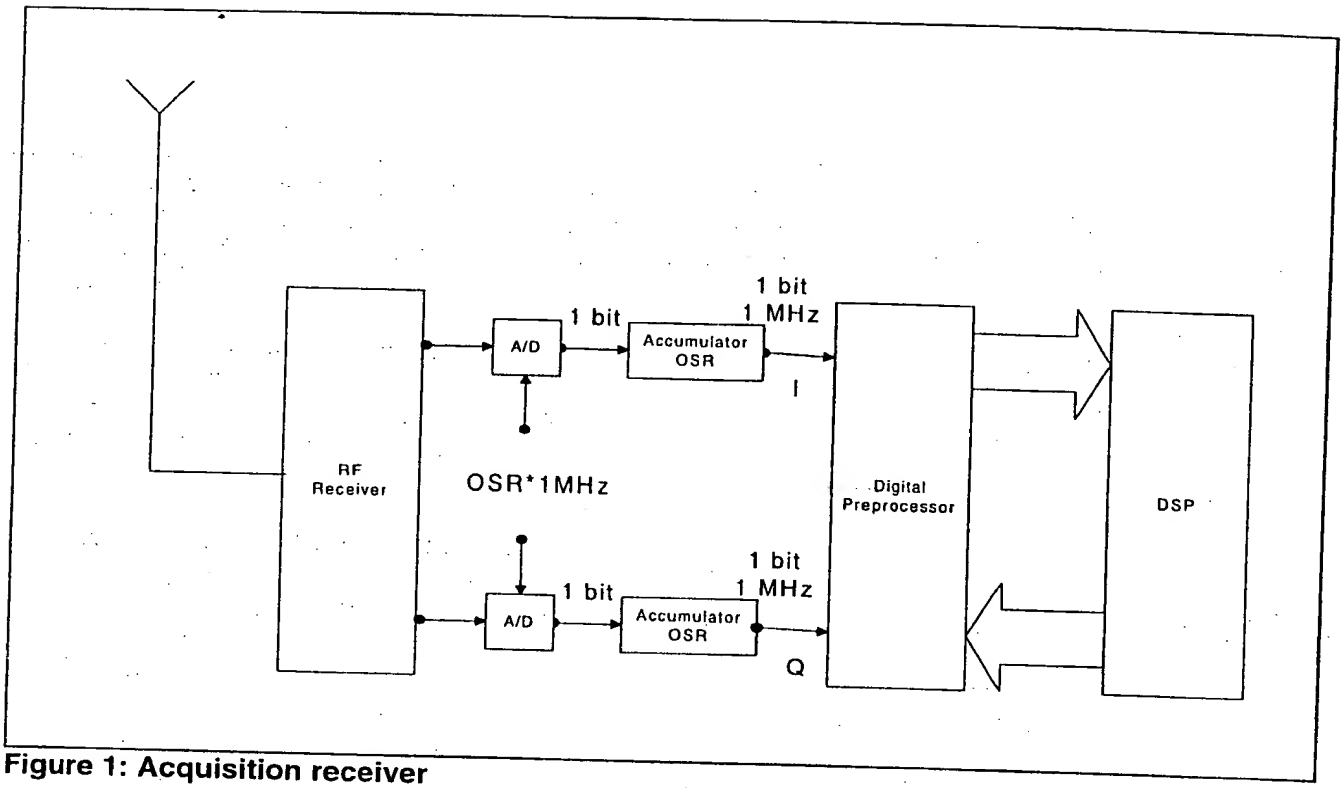


Figure 1: Acquisition receiver

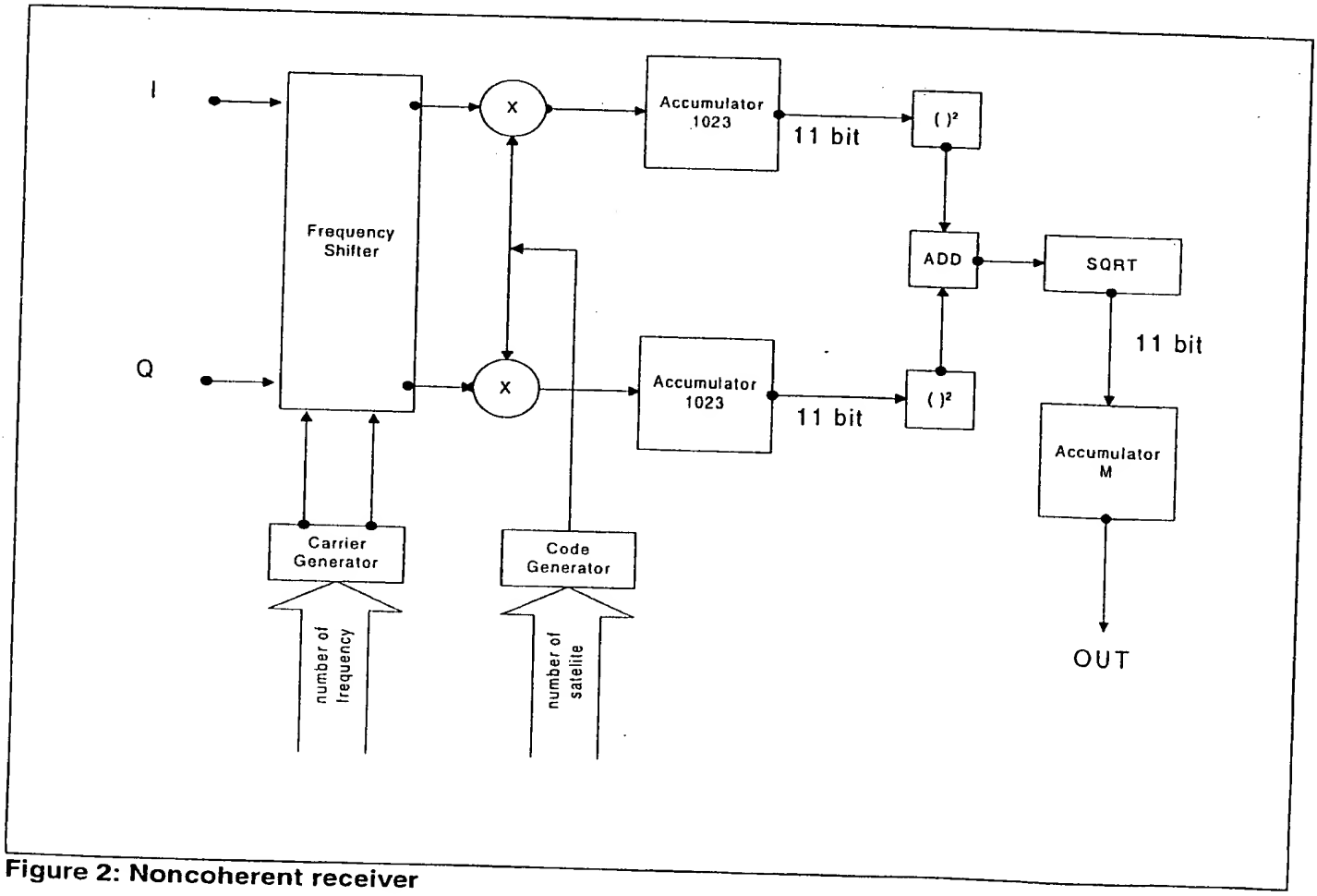


Figure 2: Noncoherent receiver

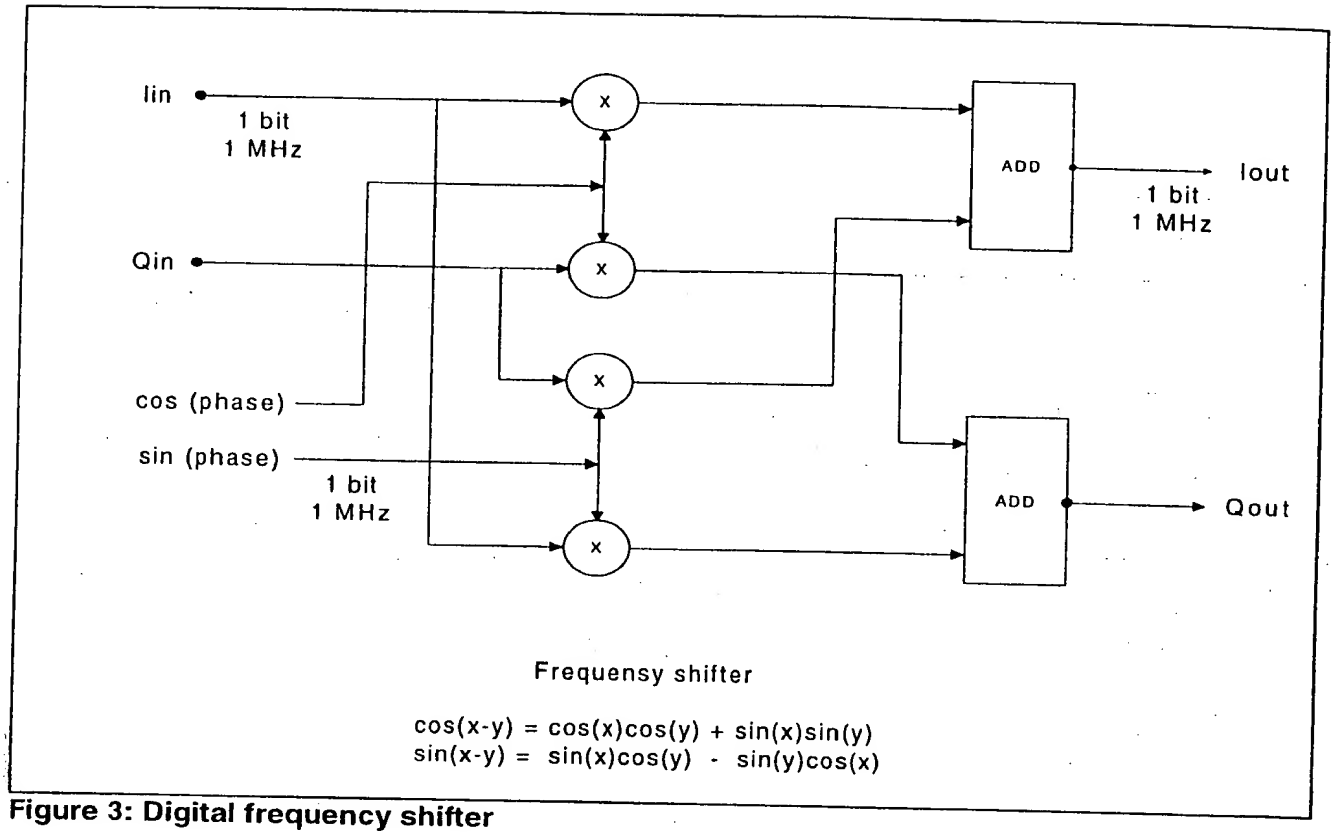


Figure 3: Digital frequency shifter

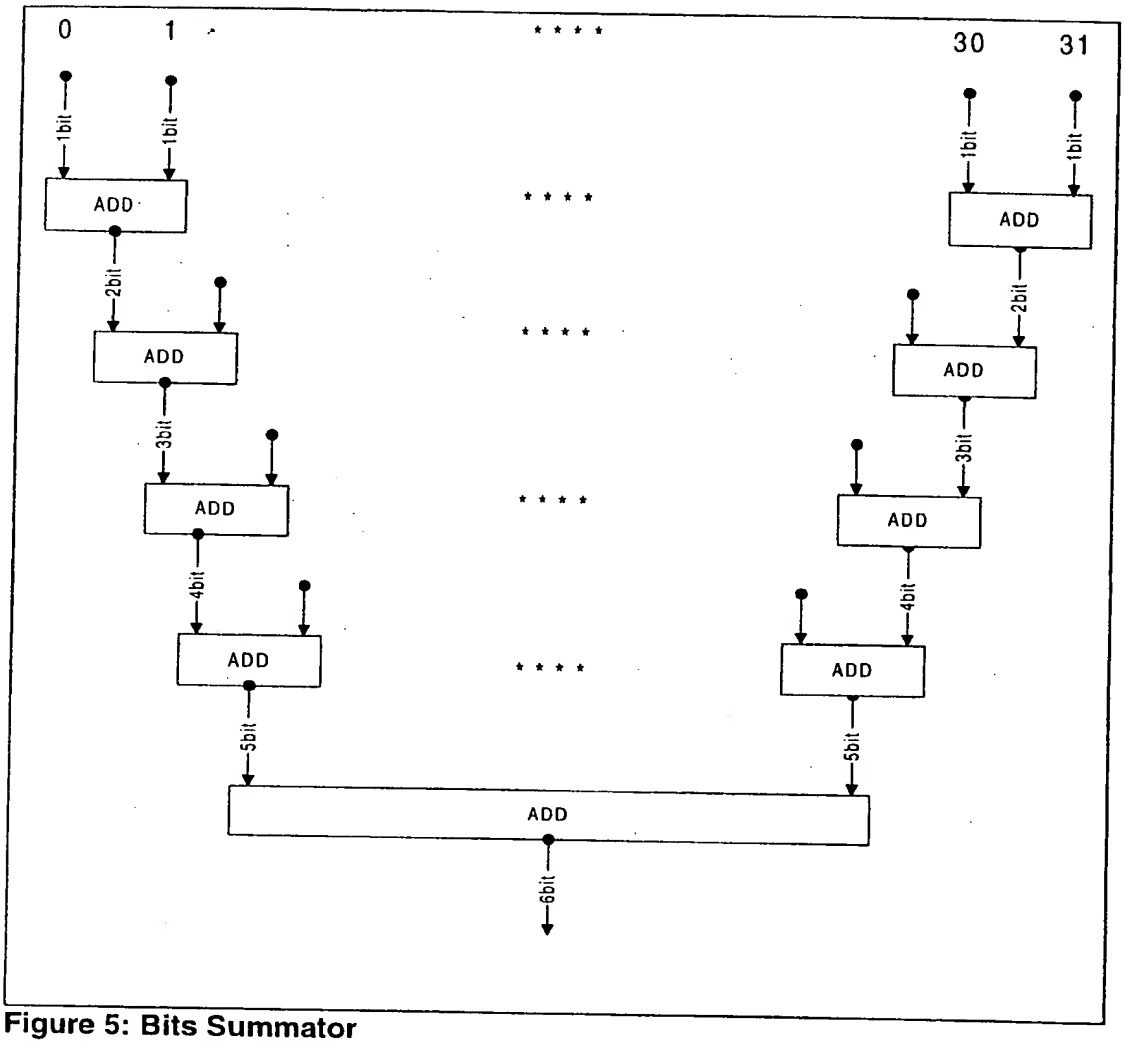


Figure 5: Bits Summator